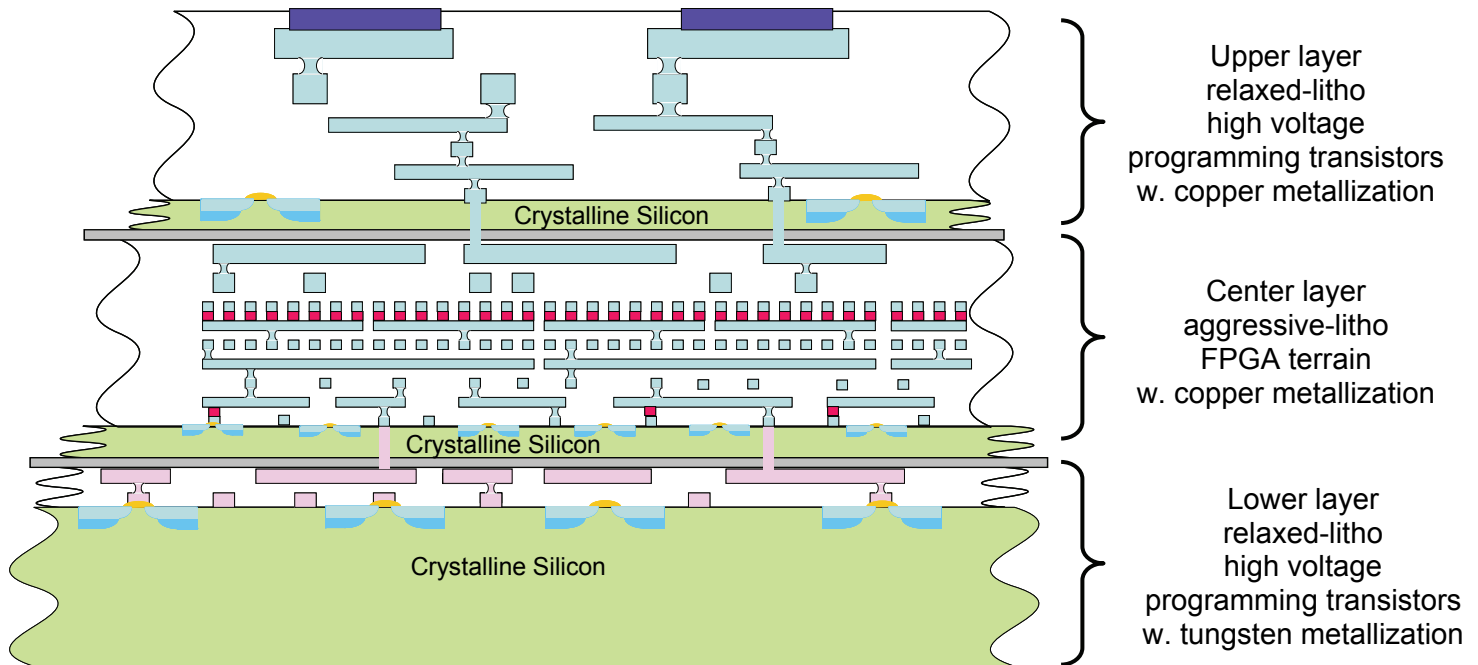


Antifuse-based 3D High Density FPGA



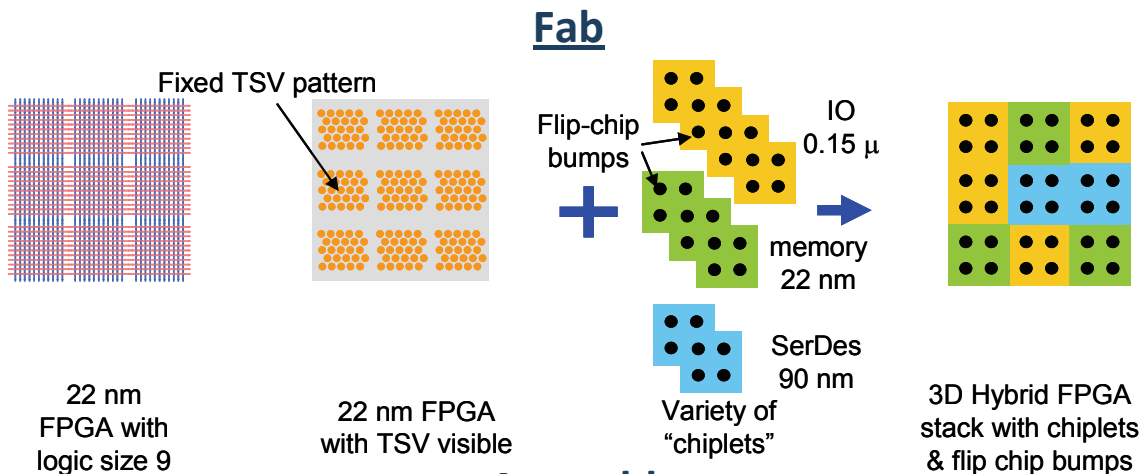
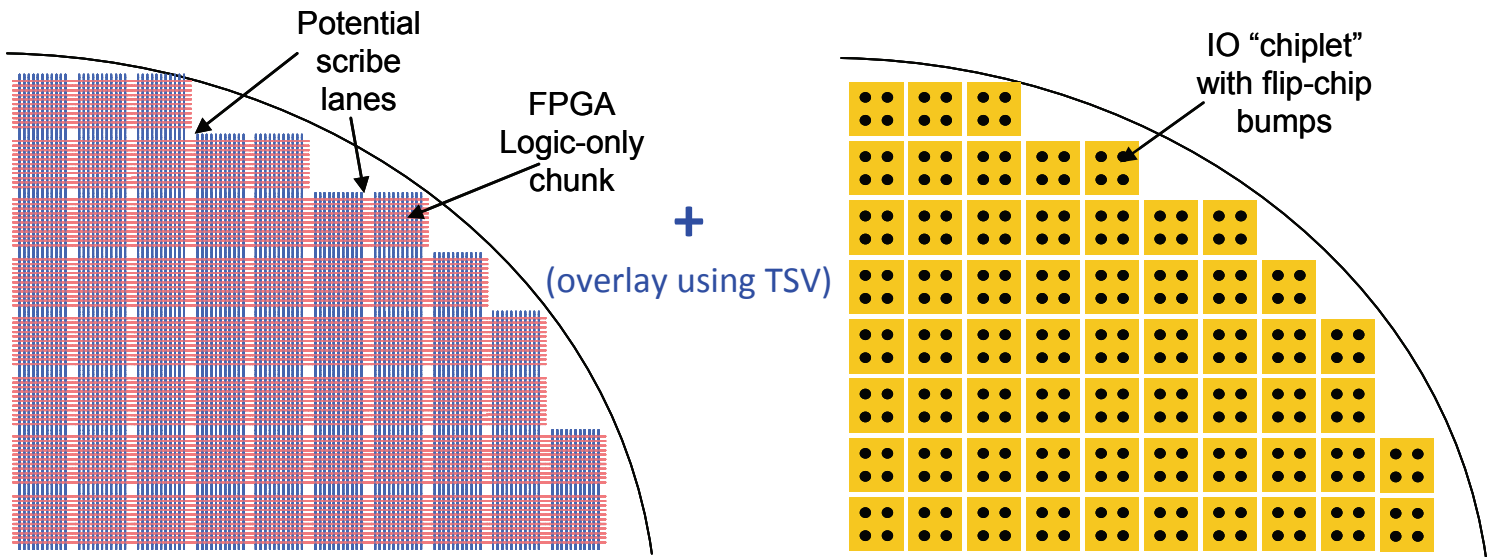
Technology:

- Antifuse-based CLB configuration
- Antifuse-based connectivity configuration
- Two layers of relaxed lithography for high voltage programming transistors
- Lower layer configures the CLB while higher-layer configures connectivity

Benefits:

- Monolithic 3D integration with novel (patent-pending) technologies. Connections between device layers are at litho feature size
- Very high density FPGA terrain uninterrupted with high-voltage programming devices
- Easy integration of high voltage and low voltage terrains
- CLB programming and interconnect programming do not cross multiple metal layers or create routing blockages
- Brings rad-hard programmable technology into nanometer lithography devices
- Programming element density approaches maximum via density
- Particularly suited to military and aerospace applications

Inexpensive Arbitrary-sized FPGA Manufacturing



Assembly

Technology:

- Wafer-scale Continuous Array
- Applicable to both antifuse and memory-based FPGAs
- Block memory can be a part of the logic terrain, separate 3D-stacked layer, or in chiplets
- TSV or microbump-based Wafer-on-Wafer and Chip-on-Wafer 3D stacking

Benefits:

- Infinitely variable FPGA family without the high cost of multiple mask sets
- Arbitrary-sized FPGA dies with a single mask set
- Inexpensive and flexible I/O configuration
- Re-use of older prequalified silicon I/O combined with the most advanced logic technology
- Large optimized memory blocks